IN THE SPECIFICATION:

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] State of the Art: Portable electronic devices require data storage, such as a memory device, for providing large storage capacity and low power consumption. To reduce power consumption and extend available power supplies, such as batteries, the memory device typically operates in a low-power mode when stored data is not being accessed. In the low-power mode, supply voltages within the memory device ~~is~~ are typically reduced to lower the power consumption of the components. While the supply voltages are varied to reduce power consumption in the low-power mode, data stored within the memory devices must be retained.

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] In typical electronic devices, large storage capacities are generally desirable. Accordingly, ~~dynamic~~ a dynamic random access memory (DRAM), which has a relatively large storage capacity over other types of memories, is frequently utilized. In a DRAM, the data is "dynamic" because the data stored within the memory cells of the memory device must be periodically recharged or "refreshed" to maintain an adequate charge to signify a specific data bit state. By way of example, a conventional DRAM device includes a plurality of memory cells arranged in rows and columns with each memory cell further including an access transistor and a storage capacitor connected in series between a digital line and a reference voltage generally equivalent to VCC/2.

Please replace paragraph number **[0011]** with the following rewritten paragraph:

[0011] In yet another embodiment, an electronic system including an input device, an output device, a memory device, and a processor device coupled to the input, output, ~~and a~~ and memory device is provided. The memory device includes a memory array having at least one memory cell configured to be periodically refreshed, control logic coupled to the memory array and responsive to mode commands from a memory controller and a circuit for reducing power

during a standby mode of the mode commands. The control logic includes a reference including at least first and second reference signals, a switching device and a first regulator. The switching device ~~including~~ includes at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle between outputting the first reference signal to outputting the second reference signal during a standby mode. The first regulator ~~coupled~~ is coupled and responsive to the switching output of the switching device, ~~the first regulator~~ and is configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] In yet a further embodiment of the present invention, an integrated circuit die is provided. The die includes a memory array having at least one memory cell configured to be periodically refreshed and control logic coupled to the memory array and responsive to mode commands from a memory controller. The die further includes a circuit for reducing power during a standby mode of the mode commands. The circuit includes a reference with at least first and second reference signals and a switching device including at least first and second switching inputs respectively coupled to the at least first and second reference signals and a switching output configured to toggle between outputting the first reference signal to outputting the second reference signal during a standby mode. The circuit further includes a first regulator coupled and responsive to the switching output of the switching device, the first regulator being configured to output a first internal operational power derived from an external operational power as regulated by one of the first and second reference signals.

Please replace paragraph number **[0014]** with the following rewritten paragraph:

[0014] In yet a further embodiment of the present invention, a method for reducing power during a standby mode of a memory device is provided. The method includes switching from a higher reference signal to a lower reference signal as an output reference signal during a

standby mode of a memory device and regulating a first lower internal ~~operation~~ operational power from an external operational power in response to the output reference signal during the standby mode. The first lower internal operational power is configured to operate at least a first portion of the memory device during a duration of the standby mode.

Please replace paragraph number **[0025]** with the following rewritten paragraph:

[0025] FIG. 1 is a functional block diagram of a memory system 200 including a memory controller 202 coupled to a memory device 204 that includes a standby mode power reduction circuit 206 for reducing power consumption on a memory device during a standby-like mode, in accordance with various embodiments of the present invention. In operation, the power reduction circuit 206 further regulates at least portions of the internal voltages down to lower levels during specific standby–like modes, an example of which are self-refresh and power-down modes. The memory device 204 in FIG. 1 is a double-data rate (DDR) synchronous dynamic random access memory ("SDRAM"), although the principles described herein are applicable to any memory device containing memory cells that must be refreshed (i.e., that store dynamic data), such as conventional DRAMs and SDRAMs, as well as packetized memory device like synchronous link DRAM ("SLDRAM") and Rambus DRAM ("RDRAM"), and are equally applicable to any integrated circuit that stores dynamic data. In the following description, certain details are set forth to provide a sufficient understanding of the invention. It will be clear to one of ordinary skill in the art, however, that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, timing protocols, and software operations have not been shown in detail or omitted entirely in order to avoid unnecessarily obscuring the invention.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

[0026] Before describing the power reduction circuit 206 in more detail, the various components of the memory device 204 will first be described. The memory controller 202 applies row, column, and bank addresses to an address register 208 over an address bus ADDR.

Typically, a row address RA and a bank address BA are initially received by the address register 208 and applied to a row address multiplexer ~~208~~ 210 and bank control logic circuit ~~210~~ 212, respectively. The row address multiplexer ~~208~~ 210 applies either the row address RA received from the address register 208 or a refresh row address RFRA received from the self-refresh counter 246 to a plurality of row address latch and decoder circuits 214A-D. The bank control logic circuit 212 activates the row address latch and decoder circuit 214A-D corresponding to either the received bank address BA or a refresh bank address RFBA from the self-refresh counter 246, and the activated row address latch and decoder circuit latches and decodes the received row address. In response to the decoded row address, the activated row address latch and decoder circuits 214A-D applies various signals to a corresponding memory bank or array 216A-D to activate a row of memory cells corresponding to the decoded row address. The data in the memory cells in the accessed row is stored in sense amplifiers coupled to the array 216A-D, which ~~also~~ also refreshes the accessed memory cells as previously described. The row address multiplexer 210 applies the refresh row address RFRA to the row address latch and ~~decoders~~ decoder circuits 214A-D and the bank control logic circuit 212 uses the refresh bank address RFBA when the memory device 204 operates in an auto-refresh or self-refresh mode of operation in response to the memory controller 202 applying an auto- or self-refresh command to the memory device 204.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] After the address register 208 via memory controller 202 has applied the row and bank addresses RA, BA, the memory controller applies a column address CA on the address bus ADDR. The address register 208 provides the column address CA to a column address counter and latch circuit 218 which, in turn, latches the column address and applies the latched column address to a plurality of column decoders 220A-D. The bank control logic circuit 212 activates the column decoder 220A-D corresponding to the received bank address BA, and the activated column decoder decodes the column address CA from the counter and latch circuit 218. Depending on the operating mode of the memory device 204, the counter and latch circuit 218

either directly applies the latched column address to the column decoders 220A-D, or applies a sequence of column addresses to the decoders starting at the column address CA provided by the address register 208. In response to the column address from the counter and latch circuit 218, the activated column decoder ~~222A-D~~ 220A-D applies decode and control signals to an I/O gating and data masking circuit 222 which, in turn, accesses memory cells corresponding to the decoded column address in the activated row of memory cells in the array 216A-D being accessed.

Please replace paragraph number **[0028]** with the following rewritten paragraph:

[0028] During data read operations, data being read from the activated array 216A-D is coupled through the I/O gating and data masking circuit 222 to a read latch 224. The I/O gating and data masking circuit 222 supplies N bits of data to the read latch 224, which then applies two N/2 bit words to a multiplexer 226. In a specific embodiment, the I/O gating and data masking circuit 222 may provide 64 bits to the read latch 224 which, in turn, provides two 32 bits words to the multiplexer 226. A data driver circuit 228 sequentially receives the N/2 bit words from the multiplexer 226 and also receives a data strobe signal DQS from a strobe signal generator 230 and a delayed clock signal CLKDEL from a delay-locked loop (DLL) circuit 232. The DQS signal has the same frequency as the CLK, CLK* signals, and is used by the controller 202 in latching data from the memory device 204 during read operations. In response to the delayed clock signal CLKDEL, the data driver circuit 228 sequentially outputs the received N/2 bit words as corresponding data words DQ that are in synchronism with rising and falling edges of the CLK signal, respectively, and also outputs the data strobe signal DQS having rising and falling edges in synchronism with rising and falling edges of the CLK signal, respectively. Each data word DQ and the data strobe signal DQS collectively define a data bus DATA coupled to the memory controller 202 which, during read operations, ~~latches the~~ latches each N/2 bit DQ word on the DATA bus responsive to the data strobe signal DQS. As will be appreciated by those of ordinary skill in the art, the CLKDEL signal is a delayed version of the CLK signal, and the DLL circuit 232 adjusts the delay of the CLKDEL signal relative to the CLK signal to ensure that the

DQS signal and the DQ words are placed on the DATA bus in synchronism with the CLK signal. The DATA bus also includes masking signals DQM0-X, which will be described in more detail below with reference to data write operations.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] A control logic and command decoder circuit 240 receives a plurality of command and clocking signals from the memory controller 202 over a control bus CONT, and generates a plurality of control and timing signals to control the components 206-238 during operation of the memory device 204. The command signals include a chip select signal CS*, a write enable signal WE*, a column address strobe signal CAS*, and a row address strobe signal RAS*, while the clocking signals include a clock enable signal CKE* and complementary clock signals CLK, CLK*, with the "*" designating a signal as being active low. The memory controller 202 drives the command signals CS*, WE*, CAS*, and RAS* to values corresponding to a particular command, such as a read, write, auto-refresh, and standby-like commands such as self-refresh and power-down commands. In response to the clock signals CLK, CLK*, the command decoder circuit 240 latches and decodes an applied command, and generates a sequence of control signals, including power reduction control signal 300, that control various components in the memory device to execute the function of the applied command. The clock enable signal CKE enables clocking of the command decoder circuit 240 by the clock signals CLK, CLK*. The command decoder circuit 240 latches command and address signals at positive edges of the CLK, CLK* signals (i.e., the crossing point of CLK going high and CLK* going low), while the input registers 236 and data ~~drivers~~ driver circuits 228 transfer data into and from, respectively, the memory device 204 in response to both edges of the data strobe signal DQS- and thus at double the frequency of the strobe signal and clock signals CLK, CLK*. For this reason the memory device 204 is referred to as a double-data-rate device, with data being transferred to and from the device at double the rate of a conventional SDRAM, which transfers data at a rate corresponding to the frequency of the applied clock signal. The detailed operation of the control logic of the command decoder circuit 240 in generating the control and

timing signals is conventional, and thus, for the sake of brevity, will not be described in more detail.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] As previously mentioned, in battery-powered electronic devices it is desirable to place the memory device 204 in a standby or low-power mode of operation when the memory controller 202 is not accessing data stored in the memory device. In the memory device 204, exemplary low-power or standby modes include self-refresh and power-down modes. To place the memory device 204 in a self-refresh mode of operation, the memory controller 202 applies a self-refresh command to the memory device. In response to the self-refresh command, the command decoder circuit 240 applies control signals to the row address multiplexer 210 and the bank control logic circuit 212 that cause the circuits to utilize the refresh row address RFRA and refresh bank address RFBA from the self-refresh counter 246 to sequentially access each row of memory cells in the memory bank or array 216A-D to thereby refresh the memory cells. The self-refresh counter 246 controls the refresh rate at which the memory cells in the arrays ~~216A-D0~~ 216A-D. The command decoder circuit 240 applies power reduction control signals 300 to power reduction circuit 206 which further reduces power levels within active portions of the memory device 204 by regulating an internal operational power VCCR 302 to portions of the circuitry to a lower voltage level. In other embodiments, other operational powers, an example of which is illustrated as VCCDLL 304, may also be separately regulated to lower operational power levels to isolated components, such as DLL circuit 232, during standby-like modes. The operation of the power reduction circuit 206 during the standby-like modes along with the structure of the power reduction circuit will now be described in more detail.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] FIG. 2 specifically illustrates a power reduction circuit 206′ configured to regulate an operational power VCCR between fully operational levels during nonstandby modes

and lower standby operational power levels during one or more standby-like modes, in accordance with an embodiment of the present invention. The power reduction circuit 206′ includes a regulator reference 306 arranged for generating at least a first reference signal 308 of a higher power level and a second reference signal 310 of a lower power level. By way of example and not limitation, FIGS. 2-5 illustrate the regulator reference 306 ~~regulator~~ as a voltage divider network comprised of resistive elements with multiple taps or access points each exhibiting varying signal levels. Other differing implementations of references having differing reference power levels are also contemplated within the scope of the present invention and a voltage divider network is not to be considered as limiting. Because of technological advancements toward smaller signal levels and faster signals, it is desirable for regulator reference signals to be stable with minimal noise that may cause contamination of the data within the memory array.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] FIG. 2 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX at a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonself-refresh mode of operation, the first reference signal 308 couples to the regulator 314 which regulates an internal operational ~~voltage~~ power VCCR 302 to a level of 2.0 volts. When a self-refresh command is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of the regulator 314 and regulates the external operational power VCCX from a level of 2.5 volts down to a level of 1.5 volts. Therefore, when a standby-like command, such as self-refresh ~~command~~ command, is received, the memory device 204 (FIG. 1) may isolate and power off certain unnecessary functionality of the memory device 204 with the power reduction circuit 206′ further reducing the power consumed by the memory device 204 by lowering the internal operational power from, for example, 2.0 volts to 1.5 volts which is within the operational ranges of the remaining functional components of the memory device 204.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] FIG. 3 specifically illustrates a power reduction circuit 206″ configured to regulate an operational power VCCR 302 according to the embodiment of FIG. 2 and is further configured to regulate another operational power VCCDLL 304, in accordance with another embodiment of the present invention. Some functional portions of the memory device 204 (FIG. 1) benefit from isolated power. By way of example and not limitation, the memory device 204 includes a DLL circuit 232 (FIG. 1) which may generate and is susceptible to switching noise that may feedback onto internal operational power VCCR 302 from circuitry coupled thereto. To mitigate noise on a power signal to noise-sensitive circuitry, the power reduction circuit 206″ further includes a means for independently regulating an external power signal to an additional isolated operational power signal consistent with the memory device operational power levels in response to the reference signal 316. In the present embodiment and by way of example and not limitation, the means for regulating the additional operational voltage is illustrated as a regulator 318 which includes a reference input for coupling with the reference signal 316 as received from the multiplexer 312. The regulator 318 further includes a regulated output which generates operational power VCCDLL 304 used for powering the DLL circuit 232 (FIG. 1).

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] FIG. 3 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX at a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonself-refresh mode of operation, the first reference signal 308 couples to regulators 314, 318 which regulate an internal operational ~~voltage~~ power VCCR 302 to a level of 2.0 volts and an additional operational ~~voltage~~ power VCCDLL 304 to a level of 2.0 volts. When a standby mode ~~command~~ command, such as a self-refresh ~~command~~ command, is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of regulators 314, 318 and ~~regulate~~ regulates the external operational

power VCCX having a level of 2.5 volts to form both an internal operational ~~voltage~~ power VCCR 302 having a level of 1.5 volts and an additional operational power VCCDLL 304 having a level of 1.5 volts.

Please replace paragraph number **[0038]** with the following rewritten paragraph:

[0038] FIGS. 4-5 illustrate other configurations of power reduction circuit 206, in accordance with other embodiments of the present invention. FIG. 4 specifically illustrates a power reduction circuit 206''' configured to regulate an operational power VCCR between fully operational levels during nonpower-down modes and lower levels during power-down ~~modes,~~ modes, in accordance with an embodiment of the present invention. The power reduction circuit 206''' includes a regulator reference 306 arranged for generating at least a first reference signal 308 of a higher power level and a second reference signal 310 of a lower power level. The power reduction circuit 206''' further includes a switching or routing device for selecting between the first reference signal 308 and the second reference signal 310. The switching device is illustrated as a multiplexer 312 having inputs for coupling with at least the first and second reference signals 308, 310, an output for multiplexing one of the inputs therethrough and one or more control inputs for coupling with the power reduction control signals 300 (FIG. 1). In the present embodiment, the power reduction control signals are illustrated as control signals 300'' and are specific to a power-down low-power mode causing the selection of a reference signal that further causes the operational power level to be reduced during the power-down mode. The power reduction circuit 206''' further comprises a means for regulating an external power signal to an operational power level consistent with the memory device operational power levels in response to a reference signal 316. In the present embodiment, the means for regulating the memory device operational voltages is illustrated as a regulator 314 which includes a reference input for coupling with the reference signal 316 from the output of multiplexer 312 and a regulated output which generates operational power VCCR 302.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] FIG. 4 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX and a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonpower-down mode of operation, the first reference signal 308 couples to the regulator 314 which regulates an internal operational ~~voltage~~ power VCCR 302 to a level of 2.0 volts. When a power-down refresh command is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of the regulator 314 and regulates the external operational power VCCX from a level of 2.5 volts down to a level of 1.5 volts. Therefore, when a standby-like command, such as a power-down ~~command~~ command, is received, the memory device 204 (FIG. 1) may isolate and power off certain unnecessary functionality of the memory device 204 with the power reduction circuit 206''' further reducing the power consumed by the memory device 204 by lowering the internal operational power from, for example, 2.0 volts to 1.5 volts which remain within the operational range of the still powered portions of memory device 204.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] FIG. 5 specifically illustrates a power reduction circuit 206'''' configured to regulate an operational power VCCR 302 according to the embodiment of FIG. 4 and is further configured to regulate another operational power VCCDLL 304, in accordance with another embodiment of the present invention. As stated, some functional portions of the memory device 204 (FIG. 1) benefit from isolated power. When the memory device 204 includes, for example, a DLL circuit 232 (FIG. 1), independent isolation of the power provided to the DLL circuit 232 may be desirable. As illustrated in FIG. 5, the power reduction circuit 206'''' further includes a means for independently regulating an external power signal level to an additional isolated operational power signal. The means for regulating the additional operational voltage is illustrated as a regulator 318 which includes a reference input for coupling with the first reference signal 308 as received from ~~the~~ the regulator reference 306. The regulator 318 further

includes a regulated output which generates operational power ~~VCC~~ VCCDLL 304 used for powering the DLL circuit 232 (FIG. 1).

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] FIG. 5 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX at a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonpower-down mode of operation, the first reference signal 308 couples to regulators 314, 318 which regulate an internal operational ~~voltage~~ power VCCR 302 to a level of 2.0 volts and an additional operational ~~voltage~~ power ~~VCC~~ VCCDLL 304 to a level of 2.0 volts. When a power-down command is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of regulator 314 and regulates the external operational power VCCX having a level of 2.5 volts to form an internal operational ~~voltage~~ power VCCR 302 having a level of 1.5 volts while retaining operational power ~~VCC~~ VCCDLL 304 having a level of 2.0 volts allowing the DLL to remain in a locked state.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

[0042] FIG. 6 is a chart illustrating the difference in consumed power of a memory device that utilizes one or more embodiments of the present invention. The chart plots the average device current as a function of the regulated internal operational power VCCR 302. While various points are plotted in relationship to the internal operational power VCCR 302, two specific points are highlighted in accordance with the specific example previously presented. The point 320 corresponds with the VCCR of approximately 2.0 volts which corresponds to the utilization of approximately 0.63 milliamps as consumed by the memory device. When the power reduction circuit in its one or more embodiments are incorporated within memory device 204 (FIG. 1) and when the memory device 204 is commanded to enter a standby-like operational mode, examples of which are self-refresh and power-down modes, the operational

power VCCR 302 is decreased to an approximate 1.5 volt level resulting in significant power savings, as illustrated by a point 322 plotted in FIG. 6.